Low Power Design (RP 4.2.26)

Review of CMOS circuits: MOS Transistor structure and device model, The CMOS inverter and other gates. (1)

Sources of power dissipation: Static power – diode leakage, sub-threshold leakage; Dynamic power dissipation – short circuit power, switching power, glitching power; degrees of freedom (4)

Supply voltage scaling approaches: Technology level- feature size scaling, threshold voltage reduction; Logic level – Transistor sizing, Multiple Vt circuits, Logic styles for low power, synthesis of Low Power CMOS circuits; Architecture level – parallelism and pipelining; Algorithms level – Transformations to exploit concurrency (10)

Switched capacitance minimization approaches: System level – Power down, system partitioning; Algorithm level – concurrency, locality, regularity, data representation; Architecture level – concurrency, signal correlation; Logic level – Transistor sizing, logic optimization; Layout level – layout optimization; Technology level – advanced packaging, SOI (10)

Special Topics: Adiabatic switching, Battery driven synthesis (3)

Limits of Power: theoretical limits, practical limits (2)